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Online: WPI, JAPIO, CLAIMS, INSPEC

(54) Abstract Title
LCD source bus

(57) An active panel of a liquid crystal display having a thin film transistor and a pixel electrode arranged in a matrix pattern has a double gate bus line. On a substrate 101, a gate bus line 113, 113a, a gate electrode 111 and a gate pad 115 are formed using a first metal such as aluminium having low electrical resistance and a second metal such as chromium having surface stability.

The adhesion between a source bus line and a gate insulator layer 117 is improved by providing a silicon layer 139, which is also used for forming the active layers of the LCD TFTs, between the source bus line and the gate insulator layer. This structure is also used for the source bus pad contact.

Fig. 8d

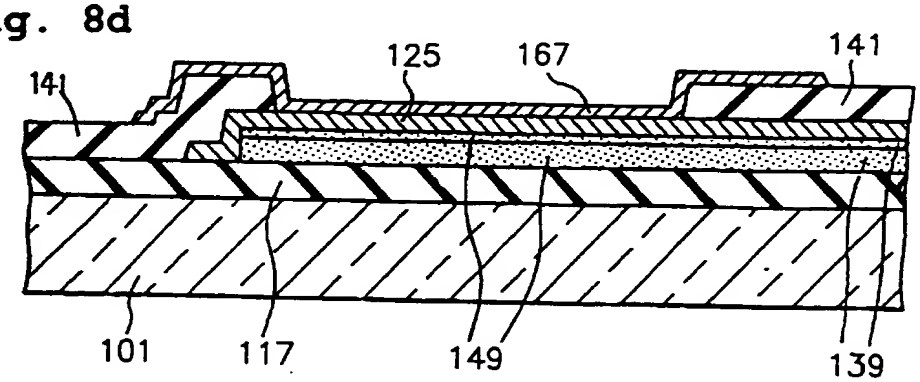

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Fig. 1
PRIOR ART

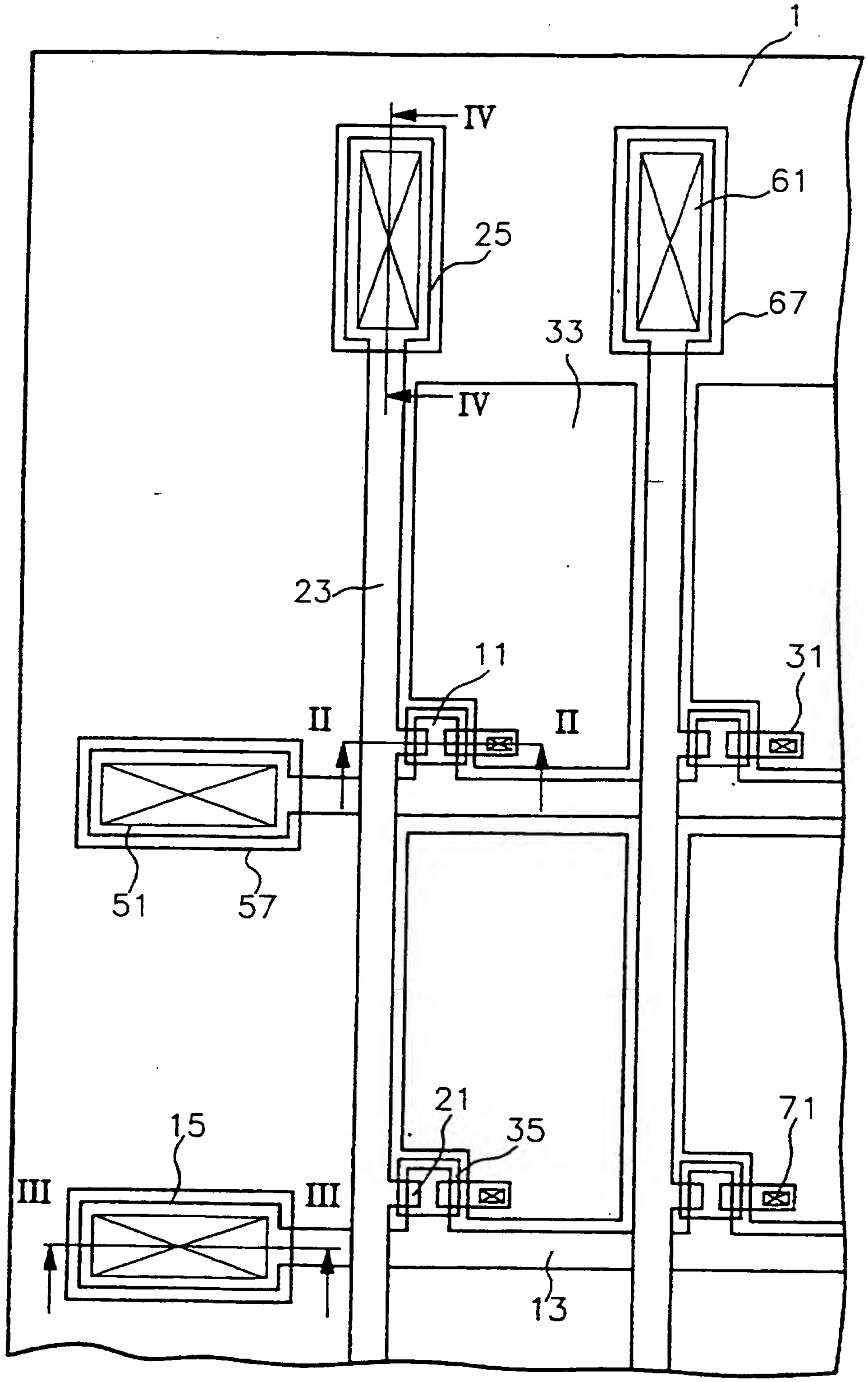


Fig. 2a
PRIOR ART

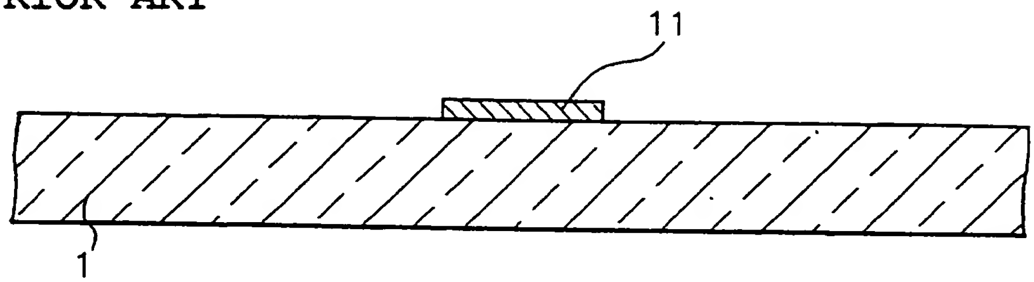


Fig. 2b
PRIOR ART

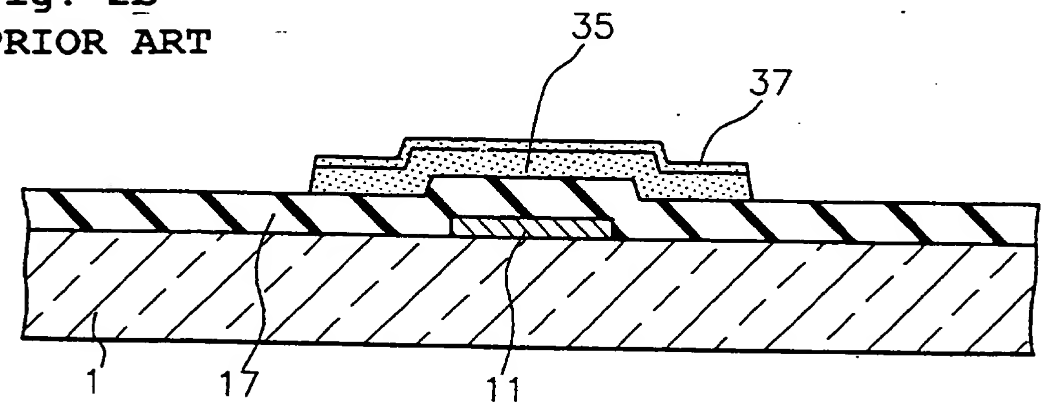


Fig. 2c
PRIOR ART

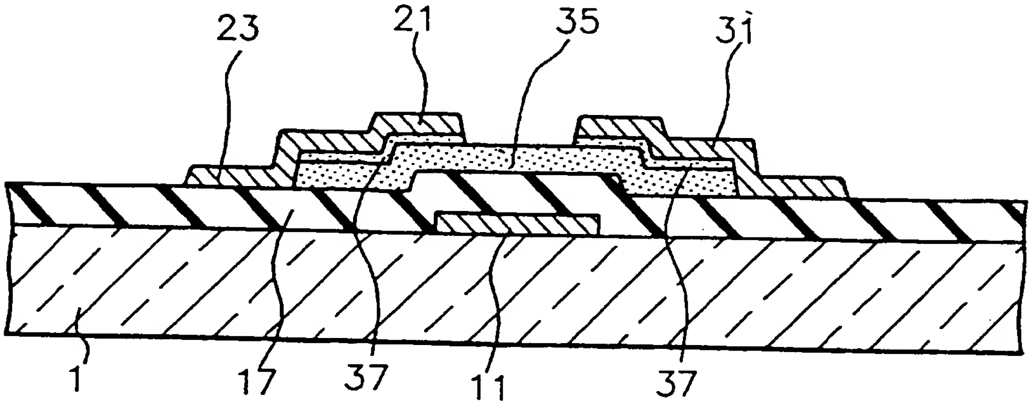


Fig. 2d
PRIOR ART

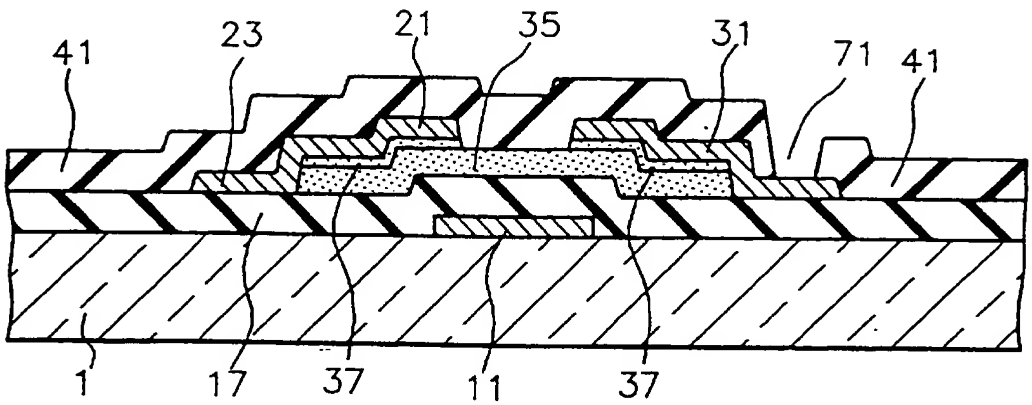


Fig. 2e
PRIOR ART

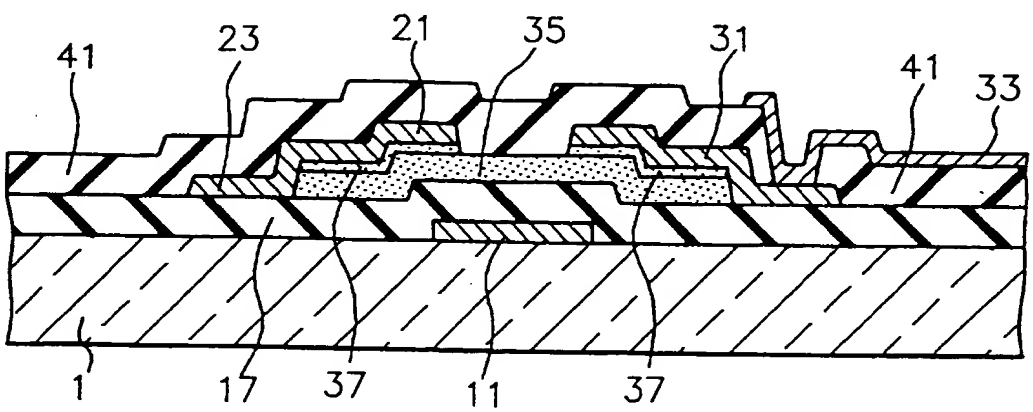


Fig. 3a
PRIOR ART

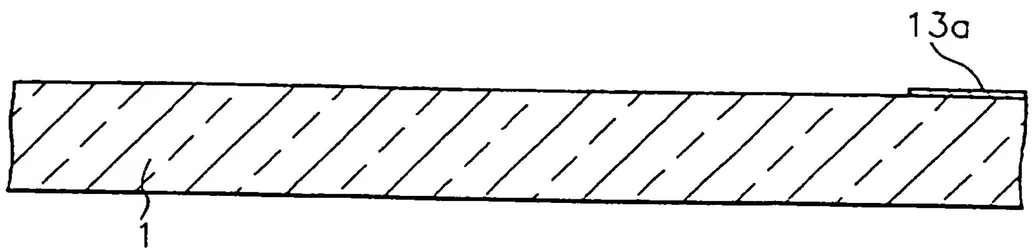


Fig. 3b
PRIOR ART

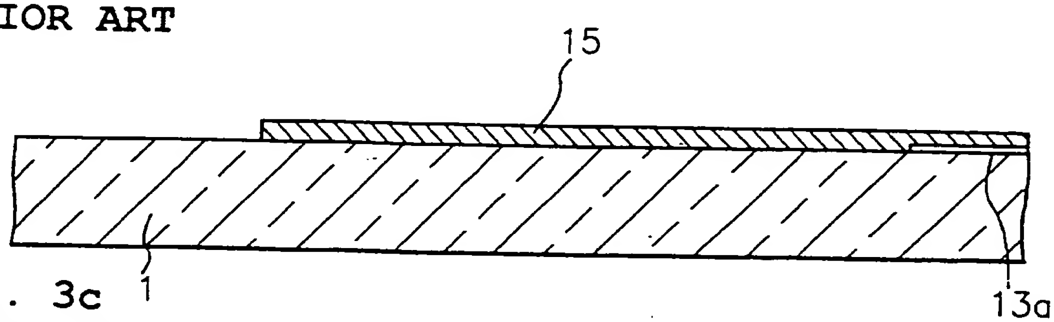


Fig. 3c
PRIOR ART

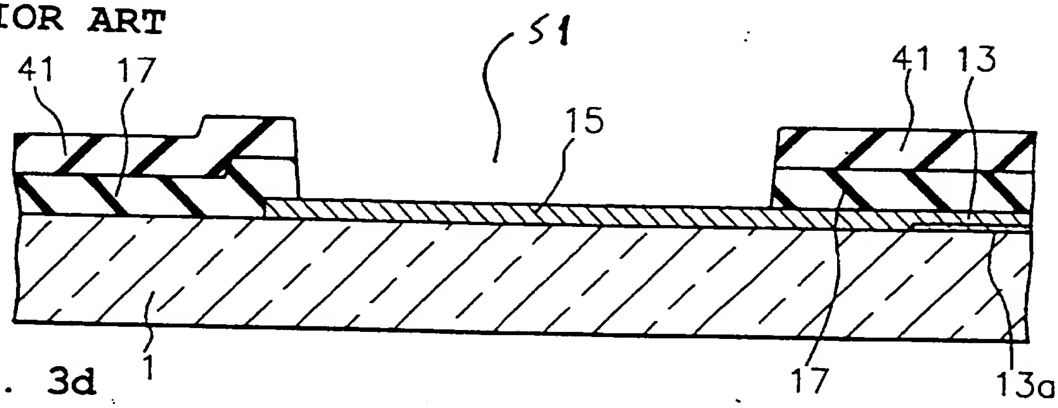


Fig. 3d
PRIOR ART

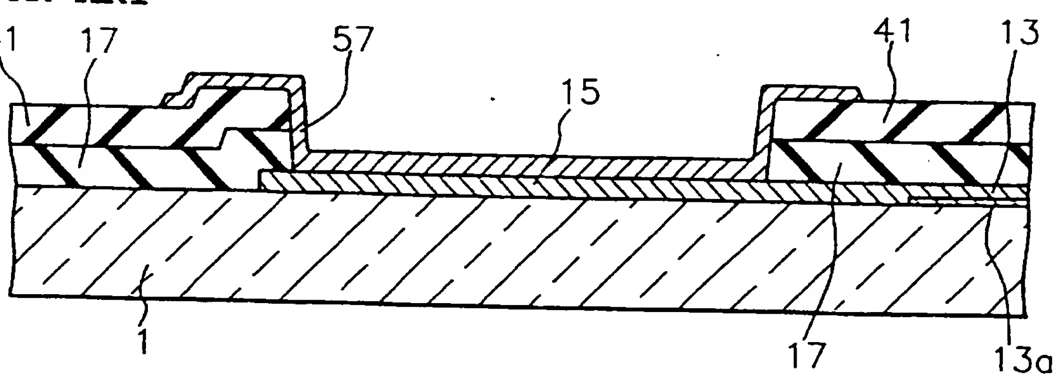


Fig. 4a
PRIOR ART

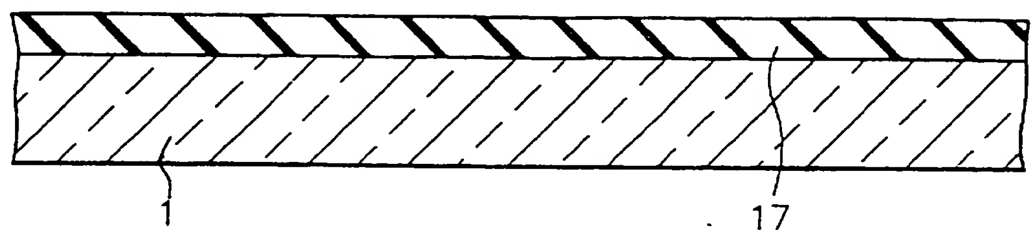


Fig. 4b
PRIOR ART

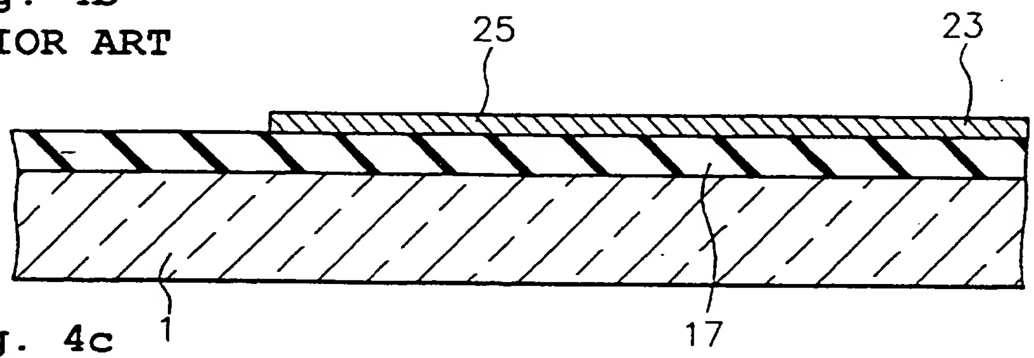


Fig. 4c
PRIOR ART

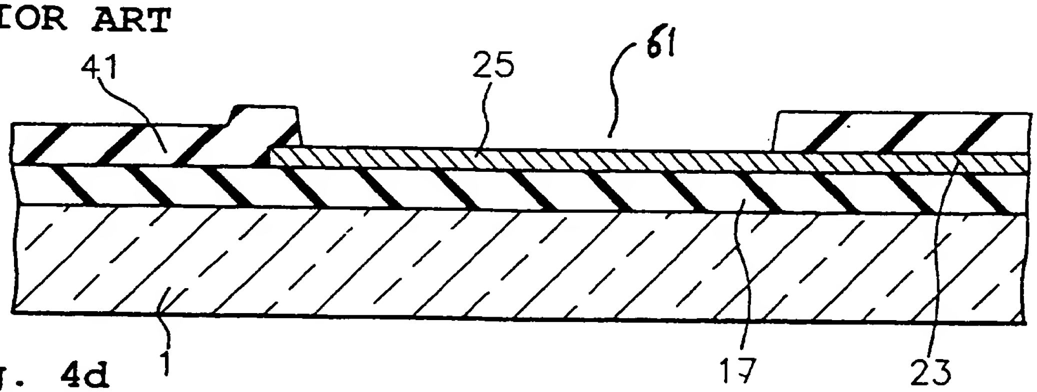


Fig. 4d
PRIOR ART

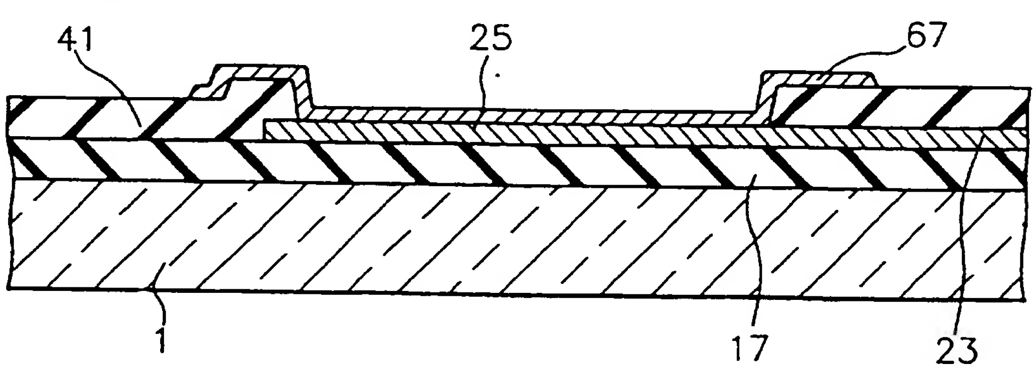
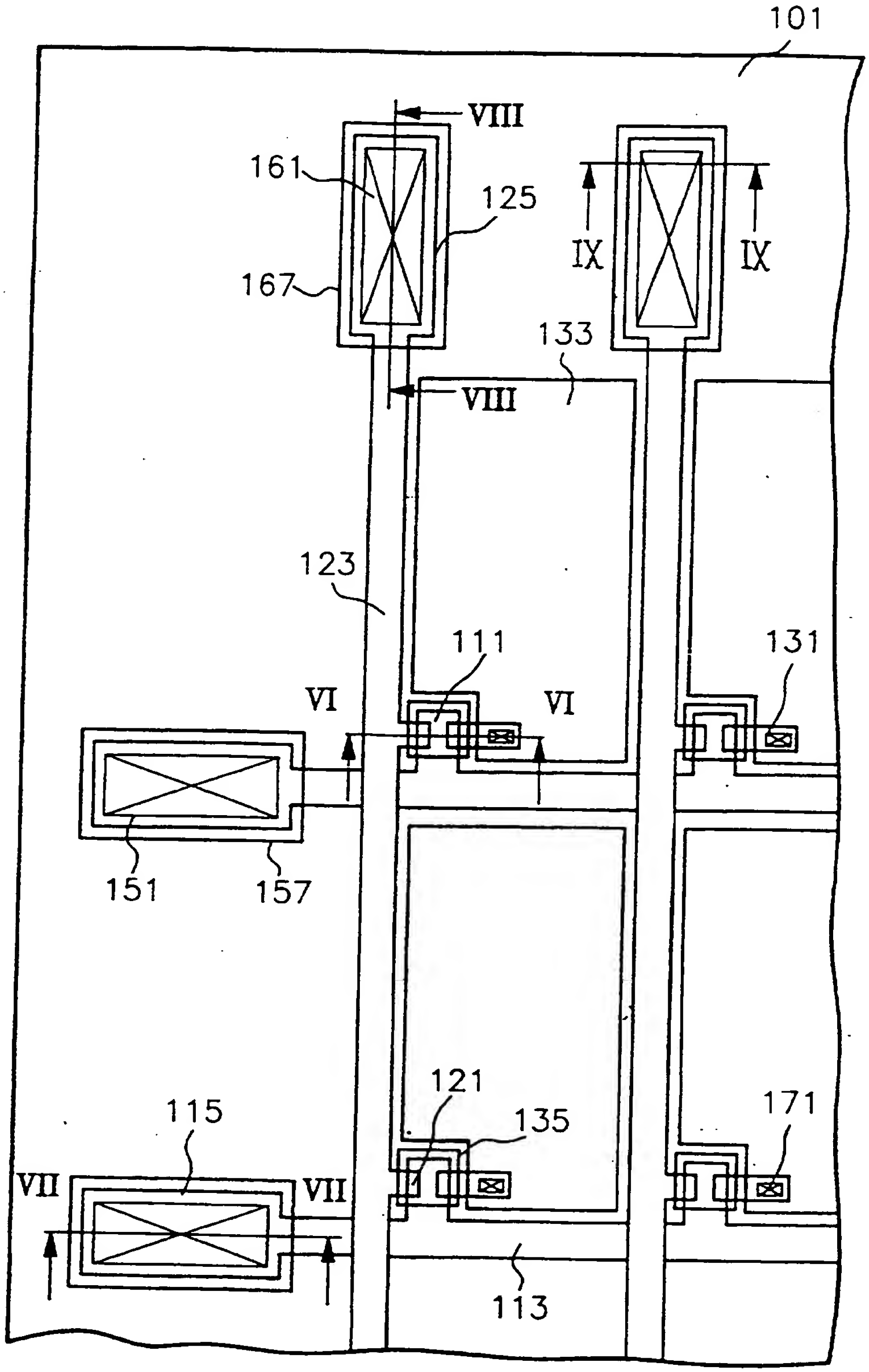


Fig. 5


101
VIII
161
125
167
IX
IX
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VIII
123
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VI
VI
151
157
121
135
171
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VII
VII
113

Fig. 6a

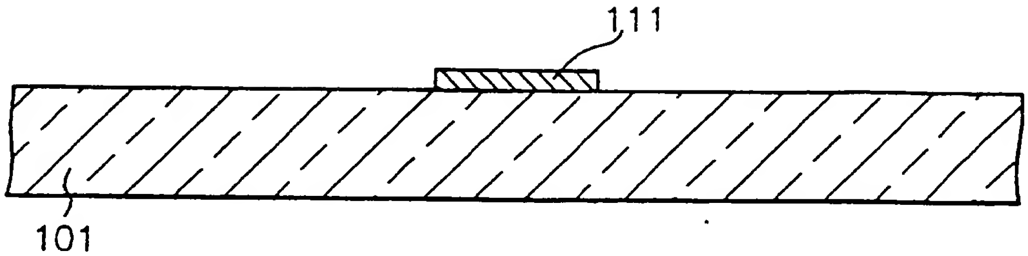


Fig. 6b

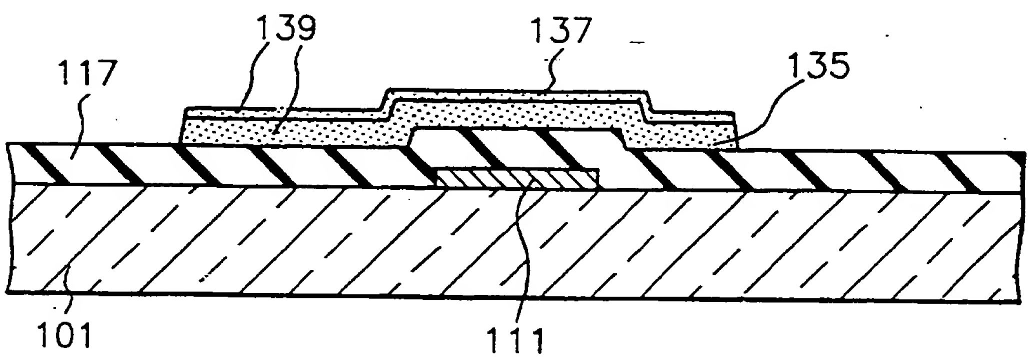


Fig. 6c

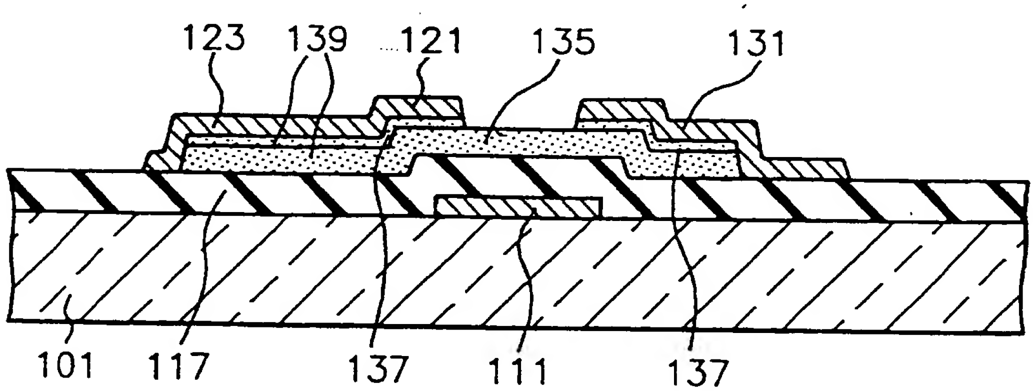
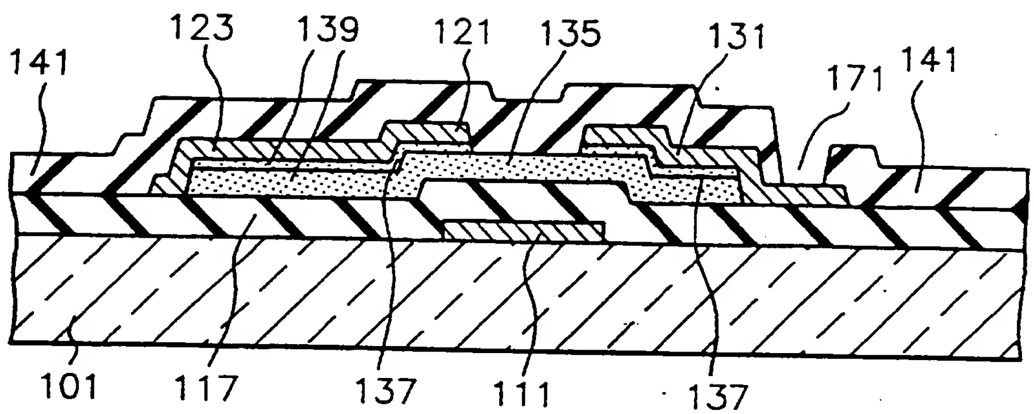


Fig. 6d


141
123
139
121
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131
171
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117
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111
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Fig. 6e

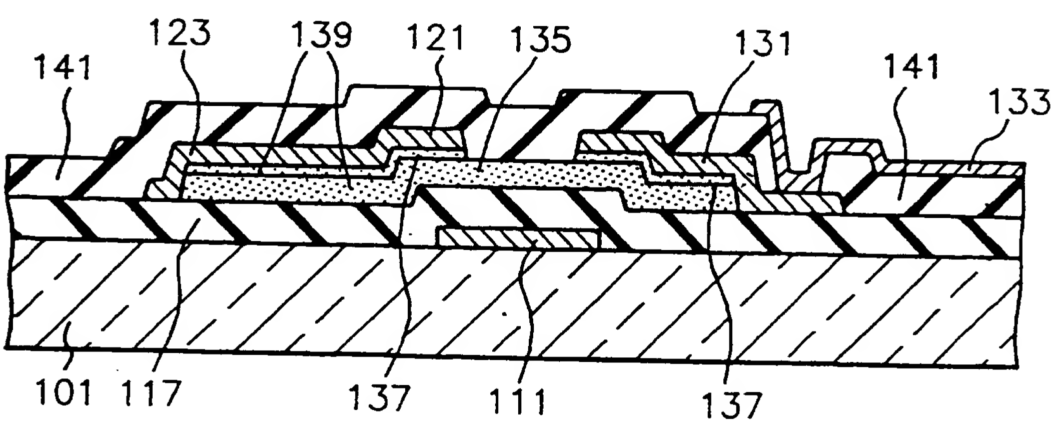
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Fig. 7a

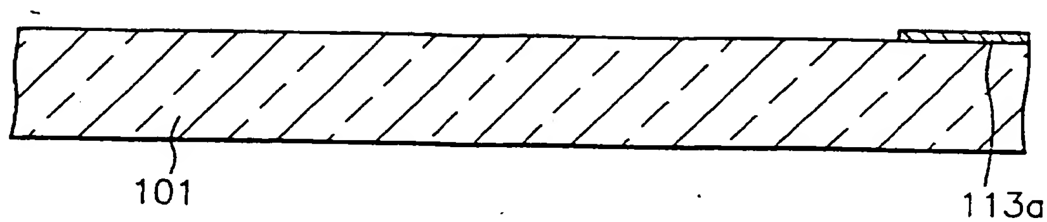


Fig. 7b

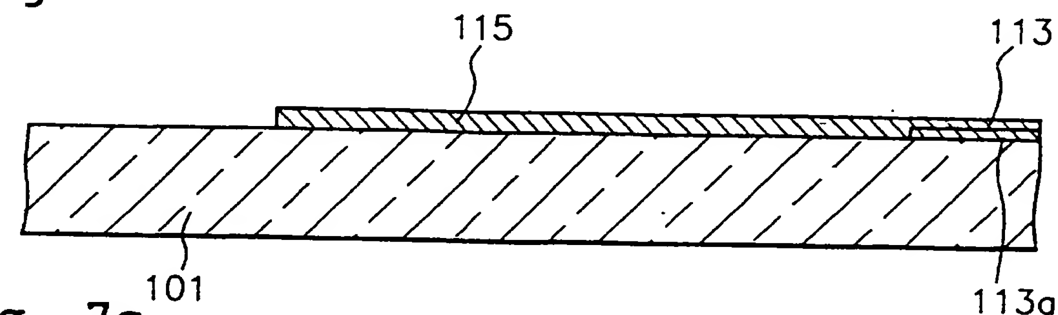


Fig. 7c

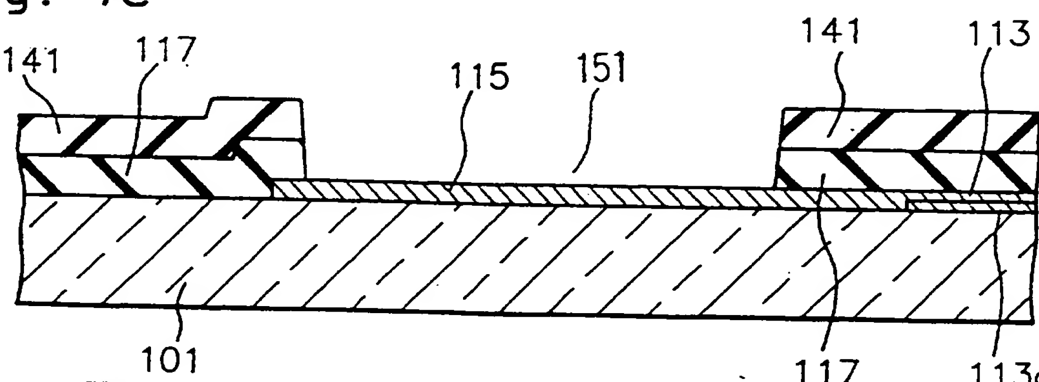
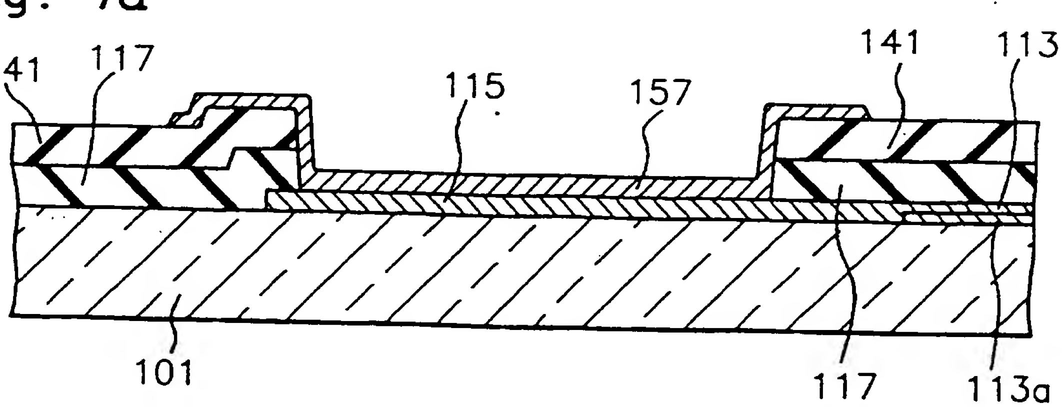


Fig. 7d



ig. 8a

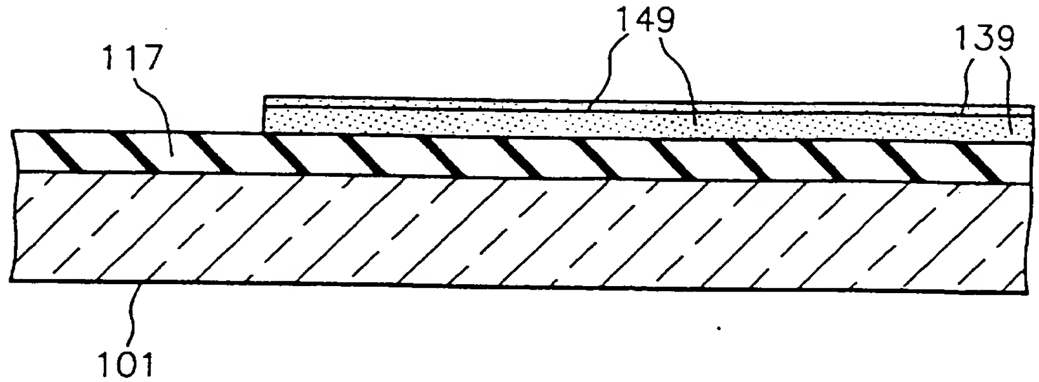


Fig. 8b

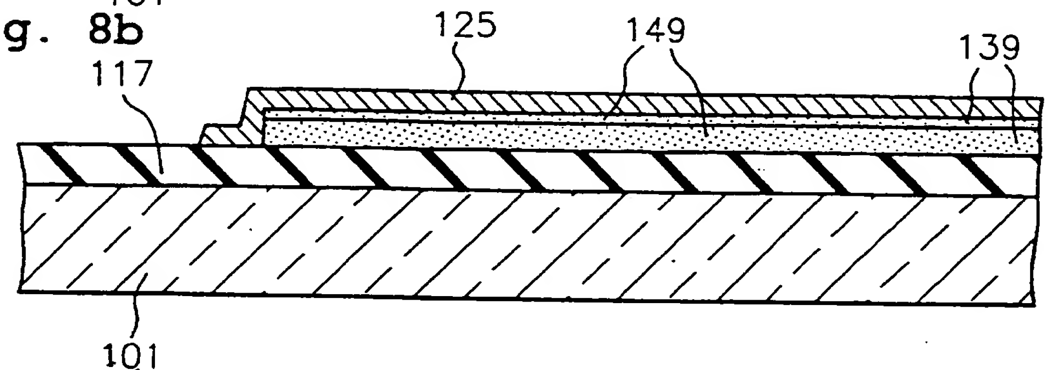


Fig. 8c

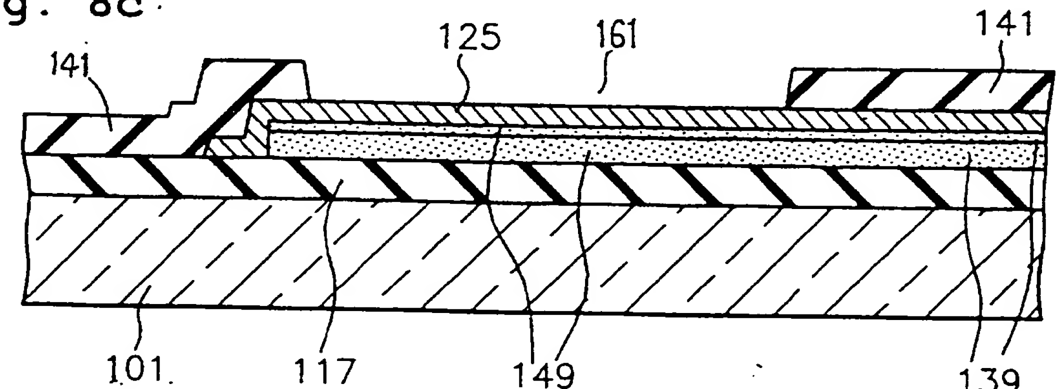


Fig. 8d

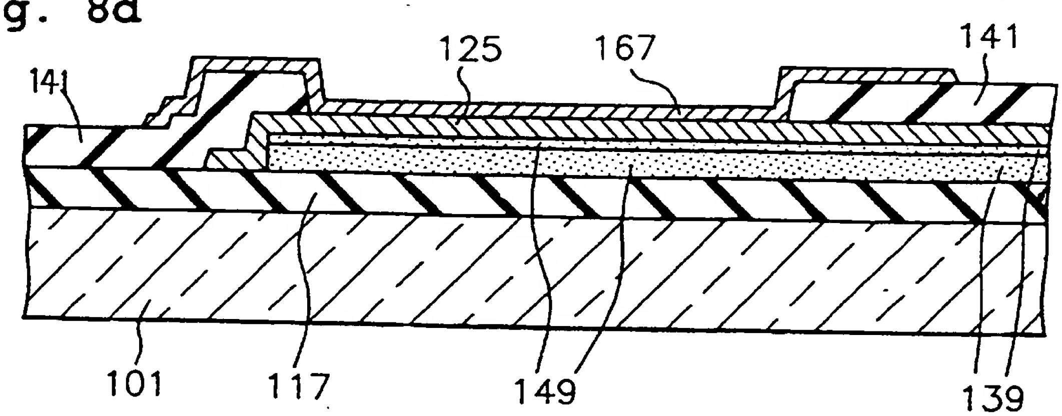


Fig. 9a

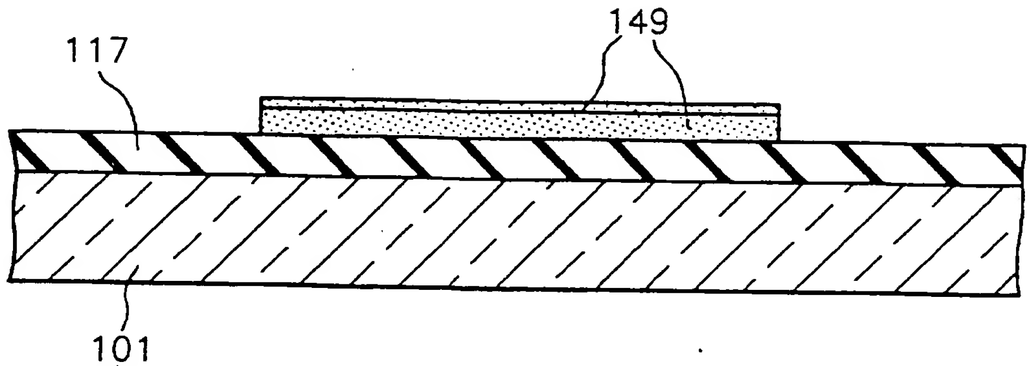


Fig. 9b

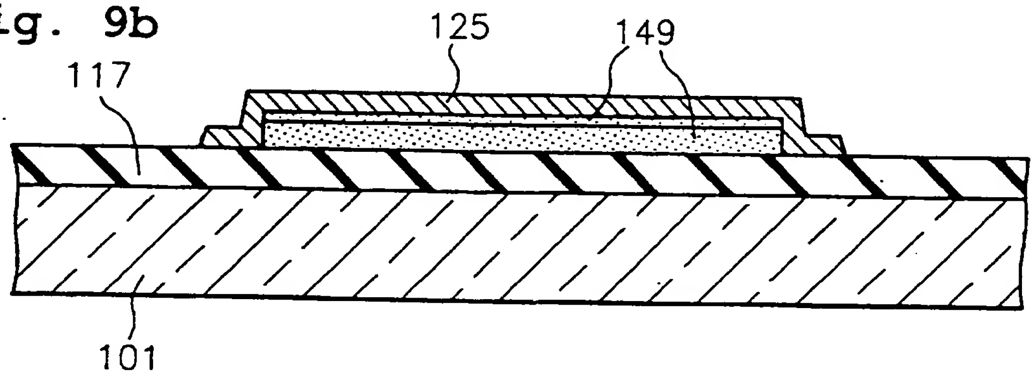


Fig. 9c

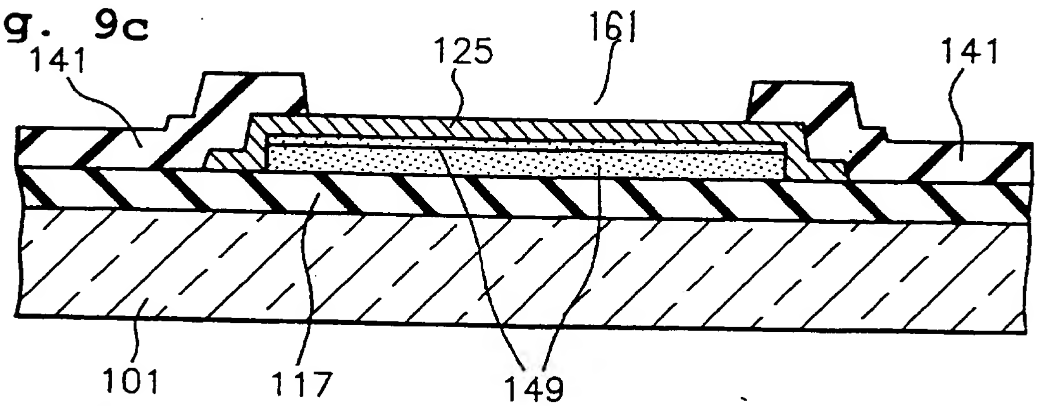


Fig. 9d

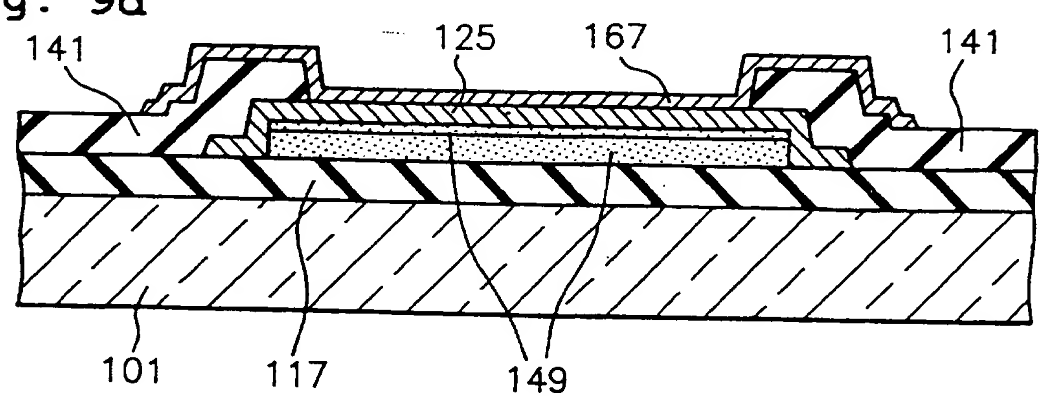


Fig. 10a

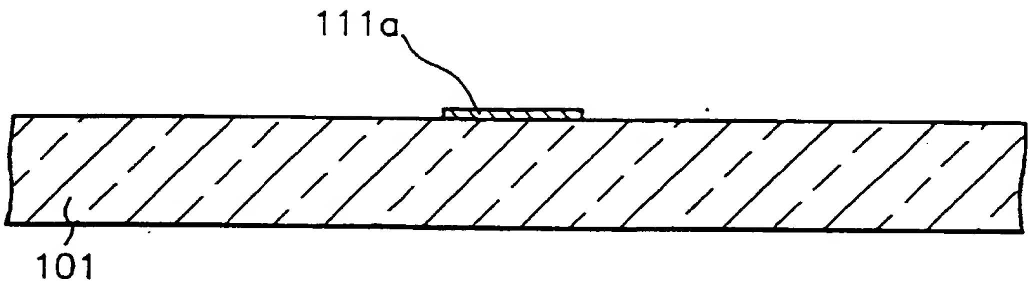


Fig. 10b

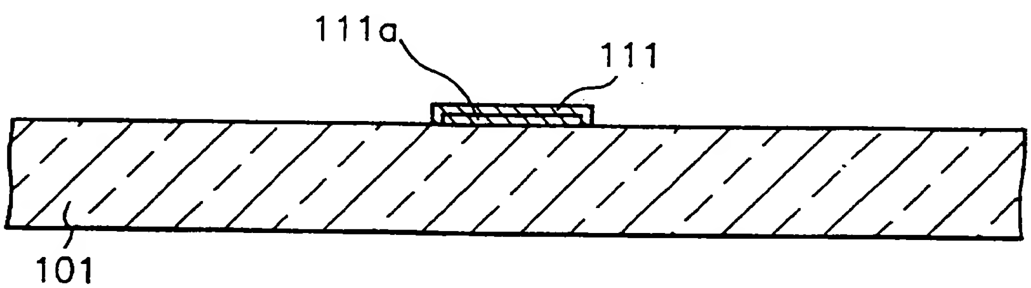


Fig. 10c

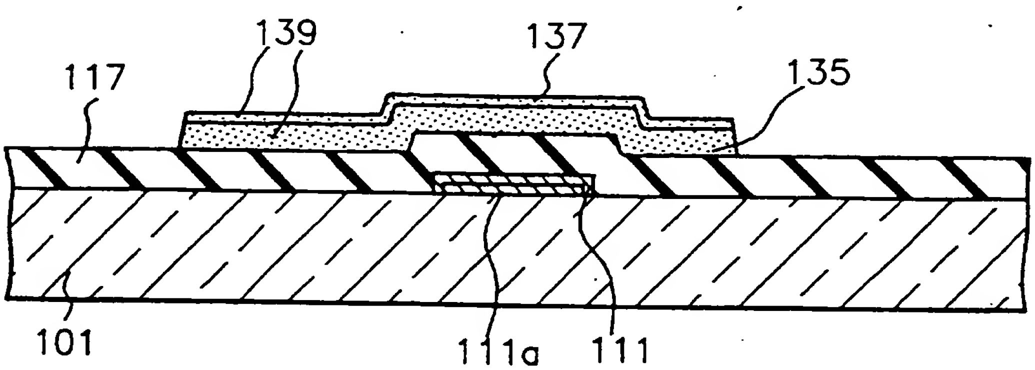


Fig. 10d

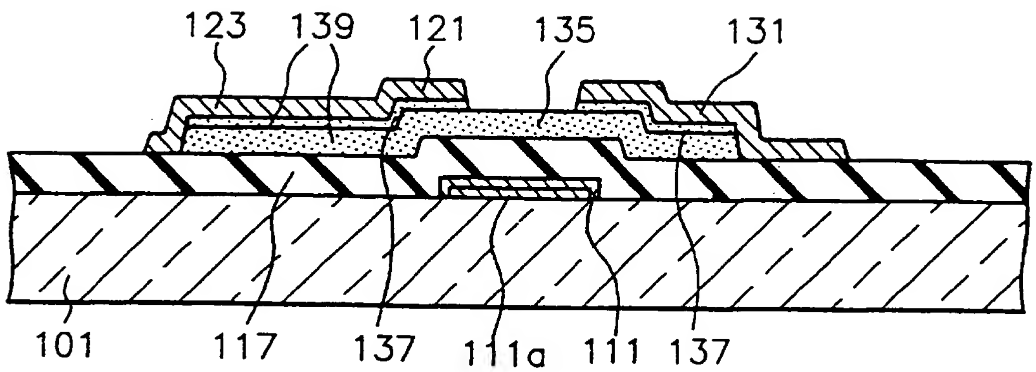


Fig. 10e

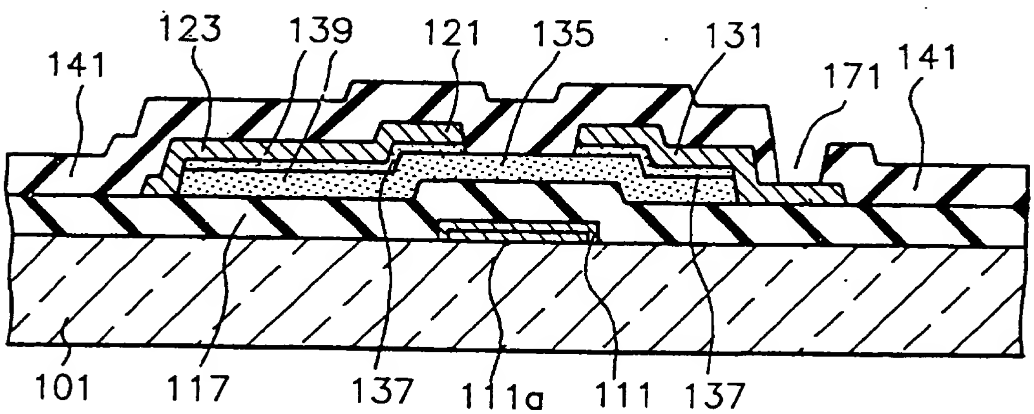


Fig. 10f

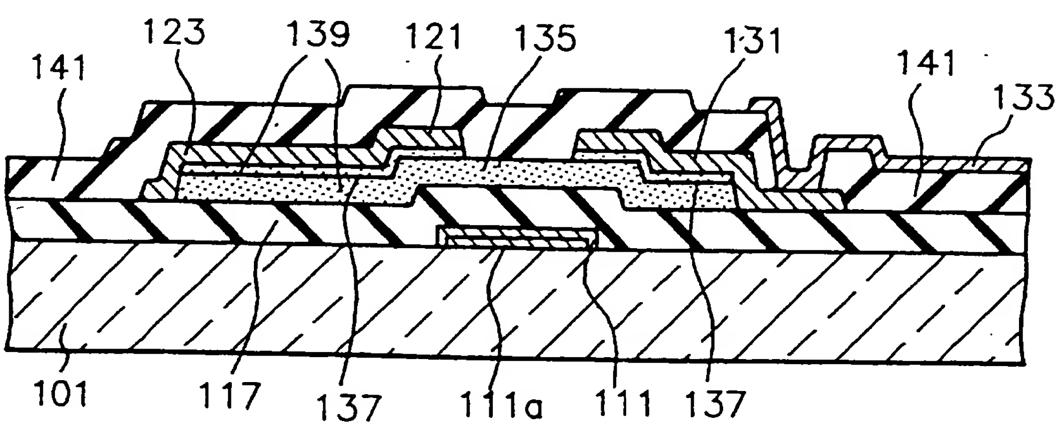


Fig. 11a

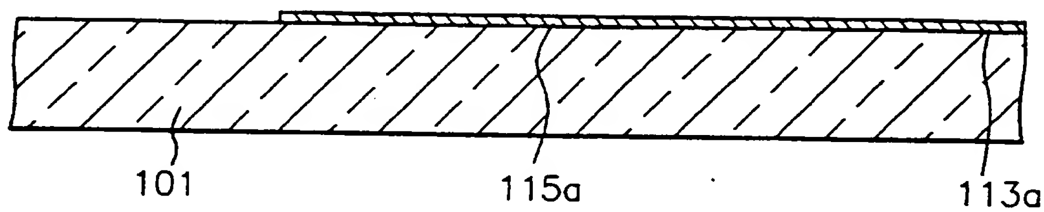


Fig. 11b

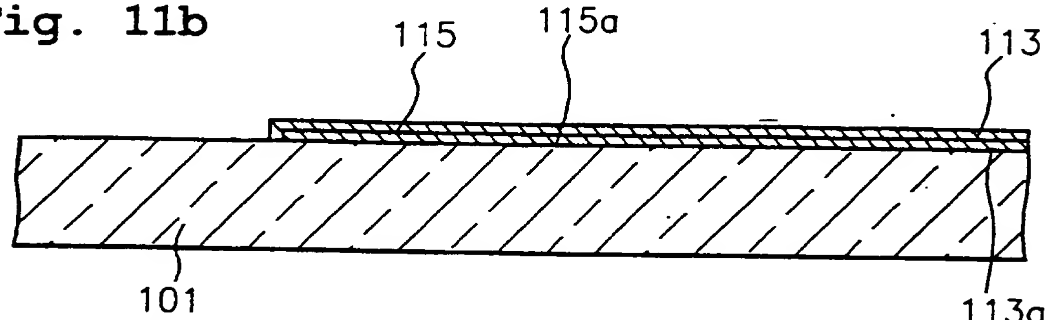


Fig. 11c

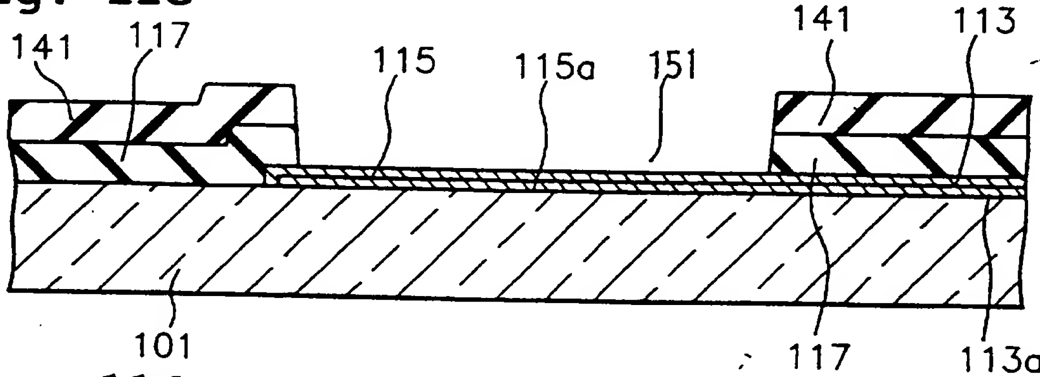
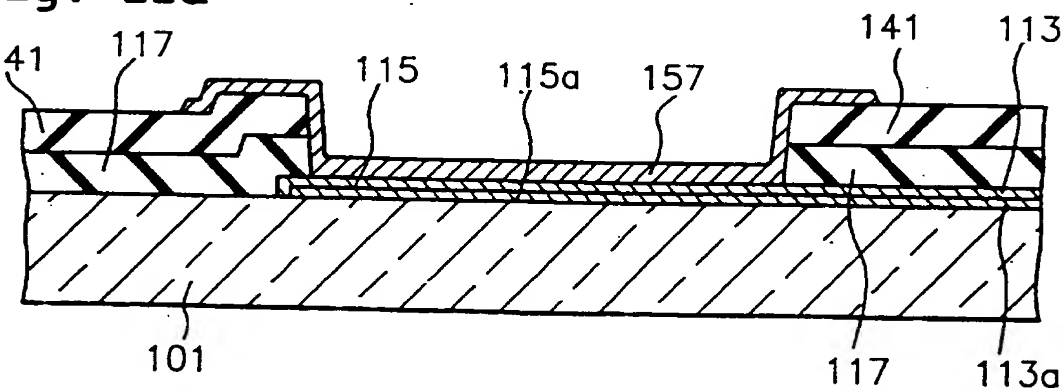


Fig. 11d



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STRUCTURE OF A LIQUID CRYSTAL DISPLAY AND A METHOD OF MANUFACTURING THE SAME

The present invention relates to an active matrix liquid crystal display (AMLCD) having active panels including thin film transistors (TFTs) and pixel electrodes arranged in a matrix pattern and a method of manufacturing the AMLCD, and more particularly but not exclusively to a method for reducing defects occurring at the source bus line and the source pad in a step of forming a double gate bus line of an AMLCD.

Among various display devices displaying images on a screen, thin film type flat panel display devices are widely used because they are relatively thin and light weight. Particularly, a liquid crystal display is actively being developed and studied because the LCD provides a sufficiently high resolution and a sufficiently fast response time to display a motion picture.

The principle of the LCD uses optical anisotrophy and polarization property of liquid crystal materials. The liquid crystal molecules are relatively thin and long having orientation and polarization properties. Using these properties, the orientation in which the liquid crystal molecules are arranged can be controlled by applying an external electric field. Depending on the orientation of the liquid crystal molecules, light is allowed to either pass through the liquid crystal or is prevented from passing through the liquid crystal. A liquid crystal display effectively uses this characteristic behavior of liquid crystal.

Recently, AMLCDs which include TFTs and pixel electrodes arranged in a matrix pattern have received much attention because they provide enhanced picture quality and natural colors.

The structure of a conventional liquid crystal display is

described below. The conventional liquid crystal display includes two panels each having many elements disposed thereon, and a liquid crystal layer formed between the two panels. The first panel (or color filter panel) located at a first side of the conventional liquid crystal display includes red (R), green (G), and blue (B) color filters sequentially arranged to correspond with an array of pixels disposed on a transparent substrate of the first panel. Between these color filters, a black matrix is arranged in a lattice pattern. A common electrode is formed and disposed on the color filters.

On the other side or second side of the conventional liquid crystal display, the second panel (or active panel) includes a plurality of pixel electrodes which are located at positions corresponding to the positions of pixels and are disposed on a transparent substrate. A plurality of signal bus lines are arranged to extend in the horizontal direction of the pixel electrodes, whereas a plurality of data bus lines are arranged to extend in the vertical direction of the pixel electrodes. At a corner of the pixel electrode, a thin film transistor is formed to apply an electric signal to the pixel. The gate electrode of the thin film transistor is connected to a corresponding one of the signal bus lines (or gate bus lines), and the source electrode of the thin film transistor is connected to a corresponding one of the data bus lines (or source bus lines). The end portions of the gate and source bus lines include terminals or pads for receiving signals applied externally thereto.

The above described first and second panels are bonded together and arranged to face each other while being spaced apart by a predetermined distance (known as a cell gap) and a liquid crystal material is injected between the two panels into the cell gap.

The manufacturing process for the conventional liquid crystal panel is rather complicated and requires many different manufacturing steps. Particularly, the active panel having TFTs

and pixel electrodes requires many manufacturing steps. Therefore, it is beneficial to reduce the manufacturing steps to reduce the possible defects which may occur during the manufacture of the active panel and to reduce the time, expense and difficulty involved in manufacturing the liquid crystal display.

In a conventional method of manufacturing an active panel, aluminum or its alloy of low electric resistance **is used** to form the gate bus line and the gate electrode and the surface of the aluminum is anodized to prevent hill-lock, thereby forming an anodic oxide film. As a result, the method required at least 8 masking steps.

However, a subsequent development in the method of manufacture has resulted in the reduction in the number of required masking steps. For example, after forming gate bus lines and gate electrodes, the surface of the aluminum is covered with a metal layer such as chromium or molybdenum instead of anodizing. Therefore, the total number of masking steps is reduced by one or two masking steps by eliminating the anodizing step and cutting the shorting bar for providing the electrode of the anodizing.

The conventional method of manufacturing the active panel is described in more detail with reference to Figs. 1-4d. Fig. 1 is a plan view showing a conventional active panel. Figs. 2a-2e are cross-sectional views showing the TFT taken along line II-II in Fig. 1. Figs. 3a-3d are cross-sectional views showing the gate pad and **gate bus line taken along line III-III in Fig.** 1. Figs. 4a-4d are cross-sectional views showing the source pad taken along line IV-IV in Fig. 1.

On a transparent substrate 1, aluminum or aluminum alloy is vacuum deposited and patterned by photo-lithography to form a low resistance gate bus line 13a (Fig. 3a). Then, chromium or chromium alloy is vacuum deposited on the surface of the aluminum or aluminum alloy including the low resistance gate bus line 13a and patterned to form a gate electrode 11 and gate pad 15 (Fig.

2a). At this time, a gate bus line 13 is formed by patterning the chromium layer to completely cover the low resistance gate bus line 13a (Fig. 3b).

Next, an insulating material such as silicon oxide (Si_xO_y) and silicon nitride (Si_xN_y) is vacuum deposited on the surface including the gate bus line 13 to form a gate insulating layer 17 (Fig. 4a). Then, a semiconductor material such as an amorphous silicon and a doped semiconductor material such as impurity doped silicon are sequentially deposited on the insulating layer 17. The semiconductor material and the doped semiconductor material are etched at all locations except for an active area above the gate electrode 11 to form a semiconductor layer 35 and a doped semiconductor layer 37 seen in Fig. 2b. In this step of removing the semiconductor material and the doped semiconductor material, the semiconductor material and the doped semiconductor material located at portions corresponding to locations where a source pad and a source bus line are to be formed, are removed.

Next, chromium or chromium alloy is vacuum deposited on the surface including the doped semiconductor layer 37 and patterned to form a source electrode 21, a drain electrode 31, a source bus line 23 and a source pad 25. The source electrode 21 and the drain electrode 31 are formed over the gate electrode 11 and separated from each other by a desired distance. Using the source electrode 21 and the drain electrode 31 as a mask, the exposed portion of the doped semiconductor layer 37 between the source 21 and drain electrode 31 is removed (Fig. 2c). The source bus line 23 connects the source electrodes 31 in a row direction (Fig. 1) and the source pad 25 is formed at the end portion of the source bus line 23 (Fig. 4b).

An insulating material such as silicon oxide and silicon nitride is vacuum deposited on the surface including the source electrode 21, drain electrode 31 and the source pad 25 to form a protection layer 41 (Fig. 2d). Then, part of the protection layer is removed by patterning to form a drain contact hole 71

(Fig. 2d). At the same time, part of the protection layer 41 covering the source pad is removed to form a source pad contact hole 61 (Fig. 4c) and part of the protection layer 41 and the gate insulating layer 17 are removed to form a gate pad contact hole 51 (Fig. 3c).

Next, indium tin oxide is vacuum deposited on the surface including the protection layer 41 and patterned to form a pixel electrode 33, a source pad connecting terminal 67 and a gate pad connecting terminal 57. The pixel electrode 33 is connected with the drain electrode 31 through the drain contact hole 71 (Fig. 2e). The source pad connecting terminal 67 is connected with the source pad 25 through the source pad contact hole 61 (Fig. 4d). The gate pad connecting terminal 57 is connected with the gate pad 15 through the gate pad contact hole 51 (Fig. 3d).

As described above, the structure of the gate pad of the active panel formed by a conventional method includes a gate pad made of aluminum and a gate pad connecting terminal made of indium tin oxide which is connected with the gate pad through a gate pad contact hole. The structure of the source pad includes a source pad made of chromium and a source pad connecting terminal made of indium tin oxide which is connected with the source pad through the source pad contact hole. Thus, since the source pad is made of chromium, during the various process steps for forming the active panel, cracks may be formed in the source pad which causes line disconnection and thereby causes defects in the active panel of the liquid crystal display.

To overcome the problems described above, the preferred embodiments of the present invention provide a liquid crystal display and a method of manufacturing a liquid crystal display for preventing line disconnection at a source pad during manufacturing to thereby reduce defects in the active panel and increase the production yield of the manufacturing process.

According to one preferred embodiment of the present

invention, a liquid crystal display includes a dummy source pad and a dummy source bus line to protect the source pad and to prevent line disconnection at the source pad.

According to another preferred embodiment of the present invention, a method of manufacturing a liquid crystal display, includes the steps of: forming a gate bus line on a substrate using a first conductive material thereon; forming an insulating layer on the substrate including the gate bus line by depositing an insulating material; forming a semiconductor layer, a doped semiconductor layer and a dummy source pad on the substrate including the gate insulating layer by depositing and patterning a semiconducting material and a doped material such as an impurity doped material; forming a source bus line and a source pad covering the dummy source pad on the substrate including the semiconductor layer, the doped semiconductor layer and the dummy source pad by depositing and patterning a second conductive material.

Further features, advantages and details of the present invention will become apparent from the detailed description of preferred embodiments provided hereafter. However, it should be understood that the description and specific examples, while indicating preferred embodiments of the invention, are given by way of illustration only, since various changes and modifications within the spirit and scope of the invention will become apparent to those skilled in the art from this detailed description.

For a better understanding of the present invention, embodiments will now be described by way of example, with reference to the accompanying drawings, in which:

Fig. 1 is an enlarged plan view showing a conventional active panel.

Figs. 2a-2e are cross-sectional views showing the manufacturing steps of forming a TFT of a conventional active panel.

Figs. 3a-3d are cross-sectional views showing the manufacturing steps of forming a gate pad and a gate bus line of a conventional active panel.

Figs. 4a-4d are cross-sectional views showing the manufacturing steps of forming a source pad and a source bus line of a conventional active panel.

Fig. 5 is an enlarged plan view showing an active panel according to a preferred embodiment of the present invention.

Figs. 6a-6e are cross-sectional views showing the manufacturing steps of forming a TFT of an active panel according to a preferred embodiment of the present invention.

Figs. 7a-7d are cross-sectional views showing the manufacturing steps of forming a gate pad and a gate bus line of an active panel according to a preferred embodiment of the present invention.

Figs. 8a-8d are cross-sectional views showing the manufacturing steps of forming a source pad and a source bus line of an active panel according to a preferred embodiment of the present invention.

Figs. 9a-9d are cross-sectional views showing the manufacturing steps of forming a source pad and a source bus line of an active panel according to a preferred embodiment of the present invention.

Figs. 10a-10f are cross-sectional views showing the manufacturing steps of forming a TFT of an active panel according to another preferred embodiment of the present invention.

Figs. 11a-11d are cross-sectional views showing the manufacturing steps of forming a gate pad and a gate bus line of

an active panel according to another preferred embodiment of the present invention.

According to preferred embodiments of the present invention, a low resistance gate bus line preferably is formed on a substrate using a first metal. A second metal layer is formed, preferably via vacuum deposition, on the substrate including the low resistance gate bus line and is patterned to form a gate electrode and a gate pad. At the same time, a gate bus line covering the low resistance gate bus line is preferably formed. An insulating material is formed, preferably via vacuum deposition, on the substrate including the gate electrode, the gate bus line and the gate pad to form a gate insulating layer. An intrinsic semiconductor material and a doped semiconductor material such as an impurity doped semiconductor material are sequentially deposited on the surface including the insulating layer and are patterned to form a semiconductor layer and a doped semiconductor layer. According to the preferred embodiments, during a step of etching the semiconductor material and the doped semiconductor material, portions of the intrinsic semiconductor material and the doped semiconductor material corresponding to locations of where a source pad and a source bus line are to be formed, are not removed but preferably remain at the positions where a source bus line and a source pad are to be formed so as to define a dummy source bus line and dummy source pad, as well as, a semiconductor layer and doped semiconductor layer covering the active area above the gate electrode. Then, a third metal is formed, preferably via vacuum deposition, on the substrate including the doped semiconductor layer, and is patterned to form a source electrode, a drain electrode, a source bus line and a source pad. An insulating material is deposited, preferably via vacuum deposition, on the substrate including the source electrode to form a protection layer. The protection layer located over the source electrode and the source pad is then

removed to form a drain contact hole and a source pad contact hole, respectively. The protection layer and the insulating layer located over the gate pad are removed to form a gate pad contact hole. A conductive material is deposited, preferably via vacuum deposition, on the substrate including the protection layer and is patterned to form a pixel electrode connected with the drain electrode through the drain contact hole, a gate pad connecting terminal connected with the gate pad through the gate pad contact hole, and a source pad connecting terminal connected with the source pad through the source pad contact hole.

The method of manufacturing an active panel according to a preferred embodiment of the present invention is described in more detail below.

Example 1

With reference to Figs. 5-9d, a first preferred embodiment of the present invention is described in more detail. Fig. 5 is a plan view of an active panel according to a preferred embodiment of the present invention. Figs. 6a-6e are cross-sectional views showing the manufacturing steps of the TFT of the active panel taken along line VI-VI in Fig. 5. Figs. 7a-7d are cross-sectional views showing the manufacturing steps of the gate pad and the gate bus line of the active panel taken along line VII-VII in Fig. 5. Figs. 8a-8d are cross-sectional views showing the manufacturing steps of the source pad and the source bus line of the active panel taken along line VIII-VIII in Fig. 5. Figs. 9a-9d are cross-sectional views showing the manufacturing steps of the source pad and the source bus line of the active panel taken along line IX-IX.

Aluminum or aluminum alloy is vacuum deposited on a transparent substrate 101 and patterned to form a low resistance gate bus line 113a which is formed at the position of a gate bus line 113 formed later (Fig. 7a).

A metal such as chromium, tantalum, molybdenum and antimony is vacuum deposited on the substrate including the low resistance

gate bus line 113a and patterned to form a gate electrode 111 and a gate pad 115 (Fig. 6a). At the same time, a gate bus line 113 made of the metal such as chromium, tantalum, molybdenum and antimony is formed to cover the low resistance gate bus line made of aluminium so as to prevent hill-lock on the surface of the aluminum. The gate pad 115 is preferably formed at the end of the gate bus line 113 (Fig. 7b).

An insulating material such as silicon oxide and silicon nitride is vacuum deposited on the substrate including the gate bus line 113 and the gate pad 115 to form a gate insulating layer 117.

Then, a semiconducting material such as intrinsic amorphous silicon and a doped semiconducting material such as impurity doped amorphous silicon are sequentially deposited on the gate insulating layer 117 and patterned to form a semiconductor layer 135 and a doped semiconductor layer 137. During the patterning step, a dummy source bus line 139 and a dummy source pad 149 are formed respectively at a location where a source bus line 123 and a source pad 125 are to be formed, preferably by allowing portions of the semiconductor material and the doped semiconductor material to remain at locations corresponding to where a source pad 149 and source bus line 123 will be formed (Fig. 6b, Fig. 8a and Fig. 9a).

Next, chromium or chromium alloy is vacuum deposited on the substrate including the doped semiconductor layer 137 and patterned to form a source electrode 121, a drain electrode 131, a source bus line 123 and a source pad 125. Here, the source electrode 121 and the drain electrode 131 are formed over the gate electrode 111 and separated from each other. The exposed portion of the doped semiconductor layer 137 between the drain electrode 121 and the source electrode 131 is removed by etching, using the source electrode 121 and the drain electrode 131 as masks (Fig. 6c). The source bus line 123 connects the source electrodes 121 in a row direction. The dummy source bus line 139 preferably made of the semiconducting materials 135 and 137 is

formed under the source bus line 123. The source pad 125 is formed at the end of the source bus line 123 and the dummy source pad 149 is formed under the source pad 125. The source bus line 123 and the source pad 125 cover the dummy source bus line 139 and the dummy source pad 149 formed thereunder, respectively (Fig. 8b and Fig. 9b).

Next, an insulating material such as silicon oxide and silicon nitride is vacuum deposited on the substrate including the source electrode 121, source bus line 123, the source pad 125 and the drain electrode 131 to form a protection layer 141. The protection layer 141 is patterned to form a drain contact hole 171 on the drain electrode 131 (Fig. 6d) and a source pad contact hole 161 on the source pad 125 (Fig. 8c and Fig. 9c). At the same time, the protection layer 141 and the gate insulating layer 117 are simultaneously removed to form a gate pad contact hole 151 on the gate pad 115 (Fig. 7c).

A transparent conductive material such as indium tin oxide is vacuum deposited on the substrate including the protection layer 141 and patterned to form a pixel electrode 133, a source pad connecting terminal 167 and a gate pad connecting terminal 157. The pixel electrode 133 is connected with the drain electrode 131 through the drain contact hole 171 (Fig. 6e). The source pad connecting terminal 167 is connected with the source pad 125 through the source pad contact hole 161 (Fig. 8d and Fig. 9d). The gate pad connecting terminal 157 is connected with the gate pad 115 through the gate pad contact hole 151 (Fig. 7d).

In this preferred embodiment, the gate pad portion includes the gate pad 115 made of aluminium and the gate pad connecting terminal 157 made of indium tin oxide and connected with the gate pad 115 through the gate pad contact hole 151. The source pad portion includes the source pad 125 preferably made of a metal which is preferably the same as the metal used to form the source bus line 123, the dummy source pad 149 made of the semiconducting materials 135 and 137 disposed under the source pad 125 and the source pad connecting terminal 167 connected with the source pad

125 through the source pad contact hole 161. Additionally, the dummy source bus line 139 made of the semiconducting material 135 and 137 is formed under the source bus line 123.

Example 2

With reference to Figs. 5, 8a-8d, 9a-9d, 10-10f and 11a-11d, a second preferred embodiment of the present invention is described in more detail. Fig. 5 is a plan view of an active panel according to a preferred embodiment of the present invention. Figs. 10a-10f are cross-sectional views showing the manufacturing steps of the TFT of the active panel taken along line VI-VI in Fig. 5. Figs. 11a-11d are cross-sectional views showing the manufacturing steps of the gate pad and the gate bus line of the active panel taken along line VII-VII in Fig. 5. Figs. 8a-8d are cross-sectional views showing the manufacturing steps of the source pad and the source bus line of the active panel taken along line VIII-VIII in Fig. 5. Figs. 9a-9d are cross-sectional views showing the manufacturing steps of the source pad and the source bus line of the active panel taken along line IX-IX. Figs. 8a-8d and 9a-9d are same as the first preferred embodiment.

Aluminum or aluminum alloy is vacuum deposited on a transparent substrate 101 and patterned to form a low resistance gate bus line 113a and a low resistance gate electrode 111a and a low resistance gate pad 115a. The low resistance gate electrode 111a preferably extends from the low resistance gate bus line 113a and is formed at a corner of a pixel arranged in a matrix pattern. The low resistance gate pad 115a is formed at an end of the low resistance gate bus line 113a, to which external voltage signal is applied (Fig. 10a and Fig. 11a).

A metal such as chromium, tantalum, molybdenum and antimony is vacuum deposited on the substrate including the low resistance gate bus line 113a, the low resistance gate electrode 111a and the low resistance gate pad 115a, and patterned to form a gate electrode 111, a gate bus line 113 and a gate pad 115. Here, the

gate bus line 113, the gate electrode 111, and the gate pad 115 made of the metal such as chromium, tantalum, molybdenum and antimony are formed to cover the low resistance gate bus line 113a, the low resistance gate electrode 111a and the low resistance gate pad 115a made of aluminum so as to prevent hill-lock on the surface of the aluminum (Fig. 10b and Fig. 11b).

An insulating material such as silicon oxide and silicon nitride is vacuum deposited on the substrate including the gate bus line 113, the gate electrode 111 and the gate pad 115 to form a gate insulating layer 117.

Then, a semiconducting material such as intrinsic amorphous silicon and a doped semiconducting material such as impurity doped amorphous silicon are sequentially deposited on the gate insulating layer 117 and patterned to form a semiconductor layer 135 and a doped semiconductor layer 137. During the patterning step, a dummy source bus line 139 and a dummy source pad 149 are formed, respectively, at locations where a source bus line 123 and a source pad 125 are to be formed, preferably by allowing portions of the semiconductor material and the doped semiconductor material to remain at locations corresponding to where a source pad 125 and source bus line 123 will be formed (Fig. 6b, Fig. 8a and Fig. 9a).

Next, chromium or chromium alloy is vacuum deposited on the substrate including the doped semiconductor layer 137 and patterned to form a source electrode 121, a drain electrode 131, a source bus line 123 and a source pad 125. Here, the source electrode 121 and the drain electrode 131 are formed over the gate electrode 111 and separated from each other. The exposed portion of the doped semiconductor layer 137 between the source electrode 121 and the drain electrode 131 is removed by etching, using the source electrode 121 and the drain electrode 131 as masks (Fig. 10d). The source bus line 123 connects the source electrodes 121 in a row direction. A dummy source bus line 139 preferably made of the semiconducting materials 135 and 137 is formed under the source bus line 123. The source pad 125 is

formed at the end of the source bus line 123 and the dummy source pad 149 is formed under the source pad 125. The source bus line 123 and the source pad 125 cover the dummy source bus line 139 and the dummy source pad 149 formed thereunder, respectively (Fig. 8b and Fig. 9b).

Next, an insulating material such as silicon oxide and silicon nitride is vacuum deposited on the substrate including the source electrode 121, source bus line 123, the source pad 125 and the drain electrode 131 to form a protection layer 141. The protection layer 141 is patterned to form a drain contact hole 171 on the drain electrode 131 (Fig. 10e) and a source pad contact hole 161 on the source pad 125 (Fig. 8c and Fig. 9c). At the same time, the protection layer 141 and the gate insulating layer 117 are simultaneously removed to form a gate pad contact hole 151 on the gate pad 115 (Fig. 11c).

A transparent conductive material such as indium tin oxide is vacuum deposited on the substrate including the protection layer 141 and patterned to form a pixel electrode 133, a source pad connecting terminal 167 and a gate pad connecting terminal 157. The pixel electrode 133 is connected with the drain electrode 131 through the drain contact hole 171 (Fig. 10f). The source pad connecting terminal 167 is connected with the source pad 125 through the source pad contact hole 161 (Fig. 8d and Fig. 9d). The gate pad connecting terminal 157 is connected with the gate pad 115 through the gate pad contact hole 151 (Fig. 11d).

In this preferred embodiment, the gate pad portion includes the gate pad 115 preferably made of aluminum and the gate pad connecting terminal 157 preferably made of indium tin oxide and connected with the gate pad 115 through the gate pad contact hole 151. The source pad portion includes the source pad 125 preferably made of a metal which is preferably the same as a metal used to form the source bus line 123, the dummy source pad 149 made of the semiconducting materials 135 and 137 disposed under the source pad 125 and the source pad connecting terminal 167 connected with the source pad 125 through the source pad

contact hole 161. Additionally, the dummy source bus line 139 made of the semiconducting material 135 and 137 is formed under the source bus line 123.

While the invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in form and details may be made therein without departing from the spirit and scope of the invention.

CLAIMS:

1. A method of manufacturing a liquid crystal display comprising the steps of:

providing a substrate;

forming a gate bus line on the substrate;

forming an insulating layer on the gate bus line;

forming a dummy source pad on the insulating layer; and

forming a source bus line and a source pad arranged to cover the dummy source pad.

2. A method of manufacturing a liquid crystal display according to claim 1, wherein the step of forming a dummy source pad includes the step of forming at least one of an intrinsic semiconductor layer and a doped semiconductor layer.

3. A method according to claim 1, wherein the step of forming the dummy source pad includes the step of forming a dummy source bus line over which the source pad is to be formed and using a material for forming the dummy source bus line which is the same as a material used for forming the dummy source pad.

4. A method according to claim 1, 2 or 3, further comprising the steps of:

forming a gate pad at an end of the gate bus line;

forming a source electrode;

forming a drain electrode at a distance from the source electrode;

forming a protection layer on the source electrode;

forming a drain contact hole on the drain electrode;

forming a source pad contact hole on the source pad;

forming a gate pad contact hole on the gate pad; and

forming a pixel electrode, a source pad connecting terminal and a gate pad connecting terminal on the protection layer.

5. A method of manufacturing a liquid crystal display comprising the steps of:

providing a substrate;

forming a first gate bus line using a first metal;

forming a second gate bus line covering the first gate bus line, a gate electrode extending from the second gate bus line and a gate pad at an end of the second gate bus line using a second metal;

forming a gate insulating layer on the gate electrode;

forming a semiconductor layer, a doped semiconductor layer and a dummy source pad on the gate insulating layer; and

forming a source electrode, a drain electrode, a source bus line and a source pad on the semiconductor layer, using a third metal.

6. A method according to claim 5, wherein the step of forming a dummy source pad includes the step of forming at least one of an intrinsic semiconductor layer and a doped semiconductor layer.

7. A method according to claim 5, wherein the step of forming the dummy source pad includes the step of forming a dummy source bus line over which the source pad is to be formed, using the same material used for forming the dummy source pad.

8. A method according to claim 5, 6 or 7, further comprising the steps of:

forming a first gate electrode extending from the first gate bus line and a first gate pad at an end of the first gate bus line;

wherein the gate electrode comprised of the second metal forms a second gate electrode covering the first gate electrode; and

wherein the gate pad comprised of the second metal forms a second gate pad covering the first gate pad.

9. A method according to claim 5, 6, 7 or 8, further comprising the steps of:

forming a protection layer on the source electrode;

forming a drain contact hole on the drain electrode;

forming a source pad contact hole on the source pad;

forming a gate pad contact hole on the gate pad; and

forming a pixel electrode, a source pad connecting terminal and a gate pad connecting terminal on the protection layer.

10. A method according to claim 5, 6, 7, 8 or 9, wherein the first metal includes aluminium.

11. A method according to claim 5, 6, 7, 8, 9 or 10, wherein the second metal includes at least one of chromium, molybdenum, tantalum and antimony.

12. A method according to claim 5, 6, 7, 8, 9, 10 or 11, wherein the third metal includes chromium.

13. A liquid crystal display comprising:

a substrate;

a gate bus line disposed on the substrate and including a first conductive material;

an insulating layer disposed on the gate bus line;

a dummy source pad disposed on the insulating layer;

a source pad including a second conductive material which is different from the first conductive material and is disposed on the dummy source pad; and

a source bus line connected to the source pad.

14. A liquid crystal display according to claim 13, further comprising:

a dummy source bus line located under the source bus line and connected with the source pad.

15. A liquid crystal display comprising:

a substrate;

a first gate bus line disposed on the substrate including a first metal;

a second gate bus line covering the first gate bus line and including a second metal;

a gate electrode extending from the second gate bus line;

a gate pad disposed at an end of the second gate bus line;

a gate insulating layer covering the gate electrode and the second gate bus line;

a semiconductor layer disposed on the gate insulating layer and including an intrinsic semiconducting material;

a doped semiconductor layer disposed on the semiconductor layer;

a dummy source bus line disposed on the gate insulating layer and including at least one of the intrinsic semiconducting material and the doped semiconducting material;

a dummy source pad disposed on the insulating layer and including at least one of the intrinsic semiconducting material and the **impurity** doped semiconducting material;

a source electrode disposed on the doped semiconductor layer and including a third metal;

a source bus line disposed on the dummy source bus line and connected with the source electrode, the source bus line including the third metal;

a source pad disposed on the dummy source pad and located at an end of the source bus line, the source pad including the third metal; and

a drain electrode located at a distance away from the source electrode.

16. A liquid crystal display according to claim 15, further comprising:

a protection layer located on the source electrode;

a source pad contact hole defined in the source pad;

a gate pad contact hole defined in the gate pad;

a source pad connecting terminal connected with the source pad through the source pad contact hole;

a gate pad connecting terminal connected with the gate pad through the gate pad contact hole; and

a pixel electrode connected with the drain electrode through the drain contact hole.

17. A liquid crystal display according to claim 15 or 16, further comprising:

a first gate electrode extending from the first gate bus line;

a first gate pad located at an end of the first gate bus line;

a second gate electrode covering the first gate electrode; and

a second gate pad covering the first gate pad.

18. A liquid crystal display according to claim 15, 16 or 17, wherein the first metal includes aluminium.

19. A liquid crystal display according to claim 15, 16, 17 or 18, wherein the second metal comprises at least one of chromium, molybdenum, tantalum and antimony.

20. A liquid crystal display according to claim 15, 16, 17, 18 or 19, wherein the third metal includes chromium.

21. A liquid crystal display, according to claim 15, 16, 17, 18, 19 or 20, wherein the pixel electrode, the gate pad connecting terminal and the source pad connecting terminal include indium tin oxide.

22. A liquid crystal display panel substrate, wherein the semiconductor layer has an extension, and the source bus line and source pad are formed on the extension.

23. A method of forming a liquid crystal display panel substrate, wherein the semiconductor layer is provided with an extension, and the source bus line and source pad are formed on the extension.

24. A method of manufacturing a liquid crystal display, substantially as hereinbefore described with reference to and/or as illustrated in any one of or any combination of Figs. 5 to 11d of the accompanying drawings.

25. A liquid crystal display substantially as hereinbefore described with reference to and/or as illustrated in any one of or any combination of Figs. 5 to 11d of the accompanying drawings.

26. A liquid crystal display panel substrate substantially as hereinbefore described with reference to and/or as illustrated in any one of or any combination of Figs. 5 to 11d of the accompanying drawings.

27. A method of forming a liquid crystal display panel substrate, substantially as hereinbefore described with reference to and/or as illustrated in any one of or any combination of Figs. 5 to 11d of the accompanying drawings.

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Databases searched:

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Other: Online:WPI,JAPIO,CLAIMS,INSPEC

Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
X	JP 7 020 490A (SANYO) See abstract.	1-23

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